INFORMATION DISCLOSURE STATEMENT BY APPLICANT(S) PTO-1449	Attorney Docket No. 2885/56	Application No. 10/009,649
	Patentee VORBACH et al.	
	Filing Date May 29, 2002	Group Art Unit 2192

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS				CLASS	SUBCLASS	FILING DATE
	4,791,603	Dec 13, 1988	Henry			
	4,992,933	Feb 12, 1991	Taylor			
	5,036,473	Jul 30, 1991	Butts et al.			
	5,055,997	Oct 8, 1991	Sluijter et al.			
	5,103,311	Apr 7, 1992	Sluijter et al.			
	5,212,777	May 18, 1993	Gove et al.			
	5,243,238	Sep 7, 1993	Kean			
	5,287,511	Feb 15. 1994	Robinson et al.			
	5,355,508	Oct 11, 1994	Kan			
	5,365,125	Nov 15, 1994	Goetting et al.			
	5,386,154	Jan 31, 1995	Goetting et al.			
	5,386,518	Jan 31, 1995	Reagle et al.			
	5,450,022	Sep 12, 1995	New			
	5,504,439	Apr 2, 1996	Tavana			
	5,600,597	Feb 4, 1997	Kean et al.			
	5,608,342	Mar 4, 1997	Trimberger			
	5,617,577	Apr 1, 1997	Barker et al.			
	5,619,720	Apr 8, 1997	Garde et al.			
	5,635,851	Jun 3, 1997	Tavana			
	5,642,058	Jun 24, 1997	Trimberger et al.			
	5,656,950	Aug 12, 1997	Duong et al.			
	5,659,785	Aug 19, 1997	Pechanek et al.			
	5,675,262	Oct 7, 1997	Doung et al.			
	5,682,491	Oct 28, 1997	Pechanek et al.			
	5,687,325	Nov 11, 1997	Chang			
	5,705,938	Jan 6, 1998	Kean			
	5,687,325	Nov 11, 1997	Chang			
	5,696,976	Dec 9, 1997	Nizar et al.			
	5,701,091	Dec 23, 2997	Kean			
	5,705,938	Jan 6, 1998	Kean			
	5,734,869	Mar 31, 1998	Chen			
	5,815,004	Sep 29, 1998	Trimberger et al.			
	5,857,109	Jan 5, 1999	Taylor			
	5,859,544	Jan 12, 1999	Norman			
	5,870,620	Feb 9, 1999	Kadosumi et al.			
	5,894,565	Apr 13, 1999	Furtek et al.			
	6,023,564	Feb 8, 2000	Trimberger			
	6,128,720	Oct 3, 2000	Pechanek et al.			
	6,145,072	Nov 7, 2000	Shams et al.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANT(S) PTO-1449	Attorney Docket No. 2885/56	Application No. 10/009,649
	Patentee VORBACH et al.	
	Filing Date May 29, 2002	Group Art Unit 2192

EXAMINER'S INITIALS				CLASS	SUBCLASS	FILING DATE
	6,178,494	Jan 23, 2001	Casselman			
	6,405,185	Jun 11, 2002	Pechanek et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	0 638 867 A2	Aug 11, 1994	EPO				

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Agarwal, A., et al., "APRIL: A Processor Architecture for Multiprocessing," Laboratory for Computer Science, MIT, Cambridge, MA, IEEE 1990, pp. 104-114.
	Almasi and Gottlieb, *Highly Parallel Computing*, The Benjamin/Cummings Publishing Company, Inc., Redwood City, CA, 1989, 3 pages (Fig. 4.1).
	Advanced RISC Machines Ltd (ARM), "AMBA - Advanced Microcontroller Bus Architecture Specification," (Document Number ARM IHI 0001C), September 1995, 72 pages.
	Alfke, Peter; New, Bernie, Xilinx Application Note, "Additional XC3000 Data," XAPP 024.000, 1994, pp. 8-11 through 8-20.
	Alfke, Peter; New, Bernie, Xilinx Application Note, "Adders, Subtracters and Accumulators in XC3000," XAPP 022.000, 1994, pp. 8-98 through 8-104.
	Alfke, Peter, Xilinx Application Note, "Megabit FIFO in Two Chips: One LCA Device and One DRAM," XAPP 030.000, 1994, pp. 8-148 through 8-150.
	Alfke, Peter, Xilinx Application Note, "Dynamic Reconfiguration," XAPP 093, November 10, 1997, pp. 13-45 through 13-46.
	Alfke, Peter; New, Bernie, Xilinx Application Note, "Implementing State Machines in LCA Devices," XAPP 027.001, 1994, pp. 8-169 through 8-172.
	Algotronix, Ltd., CAL64K Preliminary Data Sheet, April 1989, pp. 1-24.
	Algotronix, Ltd., CAL4096 Datasheet, 1992, pp. 1-53.
	Algotronix, Ltd., CHS2x4 User Manual, "CHA2x4 Custom Computer," 1991, pp.1-38.
	Allaire, Bill; Fischer, Bud, Xilinx Application Note, "Block Adaptive Filter," XAPP 055, August 15, 1996 (Version 1.0), pp. 1-10.
	Altera Application Note (73), "Implementing FIR Filters in FLEX Devices," Altera Corporation, February 1998, ver. 1.01, pp. 1-23.
	Athanas, P. (Thesis), "An adaptive machine architecture and compiler for dynamic processor reconfiguration," Brown University 1992, pp. 1-157.
	Berkeley Design Technology, Inc., Buyer's Guide to DSP Processors, 1995, Fremont, CA., pp. 673-698.
	Bittner, R. et al., "Colt: An Experiment in Wormhole Run-Time Reconfiguration," Bradley Department of Electrical and Computer Engineering, Blacksburg, VA, SPIE – International Society for Optical Engineering, Vol. 2914/187, November 1996, Boston, MA, pp. 187-194.
	Camilleri, Nick; Lockhard, Chris, Xilinx Application Note, "Improving XC4000 Design Performance," XAPP 043.000, 1994, pp. 8-21 through 8-35.
	Cartier, Lois, Xilinx Application Note, "System Design with New XC4000EX I/O Features," February 21, 1996, pp. 1-8.
	Chen, D., (Thesis) "Programmable arithmetic devices for high speed digital signal processing," U. California Berkeley 1992, pp. 1-175.
	Churcher, S., et al., "The XC6200 FastMap TM Processor Interface," Xilinx, Inc., August 1995, pp. 1-8.
	Cowie, Beth, Xilinx Application Note, "High Performance, Low Area, Interpolator Design for the XC6200," XAPP 081, May 7, 1997 (Version 1.0), pp. 1-10.
	Duncan, Ann, Xilinx Application Note, "A32x16 Reconfigurable Correlator for the XC6200," XAPP 084, July 25, 1997 (Version 1.0), pp. 1-14.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT(S) PTO-1449	Attorney Docket No. 2885/56	Application No. 10/009,649
	Patentee VORBACH et al.	
	Filing Date May 29, 2002	Group Art Unit 2192

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Ebeling, C., et al., "RaPiD – Reconfigurable Pipelined Datapath," Dept. of Computer Science and Engineering, U. Washington, 1996, pp. 126-135.
	Epstein, D., "IBM Extends DSP Performance with Mfast – Powerful Chip Uses Mesh Architecture to Accelerate Graphics, Video," 1995 MicroDesign Resources, Vol. 9, No. 16, December 4, 1995, pp. 231-236.
	Fawcett, B., "New SRAM-Based FPGA Architectures Address New Applications," Xilinx, Inc. San Jose, CA, November 1995, pp. 231-236.
	Goslin, G; Newgard, B, Xilinx Application Note, "16-Tap, 8-Bit FIR Filter Applications Guide," November 21, 1994, pp. 1-5.
	Iwanczuk, Roman, Xilinx Application Note, "Using the XC4000 RAM Capability," XAPP 031.000, 1994, pp. 8-127 through 8-138.
	Knapp, Steven, "Using Programmable Logic to Accelerate DSP Functions," Xilinx, Inc., 1995, pp. 1-8.
	New, Bernie, Xilinx Application Note, "Accelerating Loadable Counters in SC4000," XAPP 023.001, 1994, pp. 8-82 through 8-85.
	New, Bernie, Xilinx Application Note, "Boundary Scan Emulator for XC3000," XAPP 007.001, 1994, pp. 8-53 through 8-59.
	New, Bernie, Xilinx Application Note, "Ultra-Fast Synchronous Counters," XAPP 014.001, 1994, pp. 8-78 through 8-81.
	New, Bernie, Xilinx Application Note, "Using the Dedicated Carry Logic in XC4000," XAPP 013.001, 1994, pp. 8-105 through 8-115.
	New, Bernie, Xilinx Application Note, "Complex Digital Waveform Generator," XAPP 008.002, 1994, pp. 8-163 through 8-164.
	New, Bernie, Xilinx Application Note, "Bus-Structured Serial Input-Output Device," XAPP 010.001, 1994, pp. 8-181 through 8-182.
	Ridgeway, David, Xilinx Application Note, "Designing Complex 2-Dimensional Convolution Filters," XAPP 037.000, 1994, pp. 8-175 through 8-177.
	Rowson, J., et al., "Second-generation compilers optimize semicustom circuits," Electronic Design, February 19, 1987, pp. 92-96.
	Schewel, J., "A Hardware/Software Co-Design System using Configurable Computing Technology," Virtual Computer Corporation, Reseda, CA, IEEE 1998, pp. 620-625.
	Segers, Dennis, Xilinx Memorandum, "MIKE – Product Description and MRD," June 8, 1994, pp. 1-29.
	Texas Instruments, "TMS320C8x System-Level Synopsis," September 1995, 75 pages.
	Texas Instruments, "TMS320C80 Digital Signal Processor," Data Sheet, Digital Signal Processing Solutions 1997, 171 pages.
	Texas Instruments, "TMS320C80 (MVP) Parallel Processor," User's Guide, Digital Signal Processing Products 1995, 73 pages.
	Trainor, D.W., et al., "Implementation of the 2D DCT Using A Xilinx XC6264 FPGA," 1997, IEEE Workshop of Signal Processing Systems SiPS 97, pp. 541-550.
	Trimberger, S, (Ed.) et al., "Field-Programmable Gate Array Technology," 1994, Kluwer Academic Press, pp. 1-258 (and the Title Page, Table of Contents, and Preface) [274 pages total].
	Trimberger, S., "A Reprogrammable Gate Array and Applications," IEEE 1993, Proceedings of the IEEE, Vol. 81, No. 7, July 1993, pp. 1030-1041.
	Trimberger, S., et al., "A Time-Multiplexed FPGA," Xilinx, Inc., 1997 IEEE, pp. 22-28.
	Ujvari, Dan, Xilinx Application Note, "Digital Mixer in an XC7272," XAPP 035.002, 1994, p. 1.
	Veendrick, H., et al., "A 1.5 GIPS video signal processor (VSP)," Philips Research Laboratories, The Netherlands, IEEE 1994 Custom Integrated Circuits Conference, pp. 95-98.
	Wilkie, Bill, Xilinx Application Note, "Interfacing XC6200 To Microprocessors (TMS320C50 Example)," XAPP 064, October 9, 1996 (Version 1.1), pp. 1-9.
	Wilkie, Bill, Xilinx Application Note, "Interfacing XC6200 To Microprocessors (MC68020 Example)," XAPP 063, October 9, 1996 (Version 1.1), pp. 1-8.
	XCELL, Issue 18, Third Quarter 1995, "Introducing three new FPGA Families!"; "Introducing the XC6200 FPGA Architecture: The First FPGA Architecture Optimized for Coprocessing in Embedded System Applications," 40 pages.
	Xilinx Application Note, Advanced Product Specification, "XC6200 Field Programmable Gate Arrays," June 1, 1996 (Version 1.0), pp. 4-253 – 4-286.
	Xilinx Application Note, "A Fast Constant Coefficient Multiplier for the XC6200, XAPP 082, August 24, 1997 (Version 1.0), pp. 1-5.
	Xilinx Technical Data, "XC5200 Logic Cell Array Family," Preliminary (v1.0), April 1995, pp. 1-43.
	Xilinx Data Book, "The Programmable Logic Data Book," 1996, 909 pages.
	Xilinx, Series 6000 User's Guide, June 26, 1997, 223 pages.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT(S) PTO-1449	Attorney Docket No. 2885/56	Application No. 10/009,649
	Patentee VORBACH et al.	
	Filing Date May 29, 2002	Group Art Unit 2192

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Yeung, K., (Thesis) "A Data-Driven Multiprocessor Architecture for High Throughput Digital Signal Processing," Electronics Research Laboratory, U. California Berkeley, July 10, 1995, pp. 1-153.
	Yeung, L., et al., "A 2.4GOPS Data-Driven Reconfigurable Multiprocessor IC for DSP," Dept. of EECS, U. California Berkeley, 1995 IEEE International Solid State Circuits Conference, pp. 108-110.
	ZILOG Preliminary Product Specification, "Z86C95 CMOS Z8 Digital Signal Processor," 1992, pp. 1-82.
	ZILOG Preliminary Product Specification, "Z89120 Z89920 (ROMless) 16-Bit Mixed Signal Processor," 1992, pp. 1-82.
	Defendants' Invalidity Contentions in *PACT XPP Technologies, AG v. XILINX, Inc., et al., (E.D. Texas Dec. 28, 2007) (No. 2:07cv563)*., including Exhibits A through K in separate PDF files.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.